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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,321	01/14/2000	Gary L. Swoboda	TI-28937	8221

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EXAMINER
MAKHDOOM, SAMARINA

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/483,321	Applicant(s) SWOBODA, GARY L.
	Examiner Samarina Makhdoom	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The specification is objected to because of the following informalities: The header "TI-28937 2/19/99" should be removed from every page of the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhattacharya, U.S. Patent No. 6,378,090.

As per Claim 1, Bhattacharya discloses a method for emulation communications via a test access port and boundary-scan architecture providing serial access to a serial connection of a plurality of registers disposed in a plurality of modules, comprising the steps of:

selecting for communication one of said plurality of modules, nonselected module being nonresponsive to data on said serial connection (See Figure 3, for a plurality of cores or modules with test access ports in a single integrated circuit in which the plural test access ports are serially connected. See Col. 4, lines 48 et Seq. for the disclosure of the non-TAPed cores 310 (or nonselected modules) are connected to the first test port are nonresponsive to data of the serial connection);

supplying to the test access port for communication to the boundary-scan architecture a serial signal having a first logic state for a number of cycles greater in number than a number of bits of the serial connection of the plurality of registers (See the Abstract for the disclosure of a test access port for communication to a boundary-scan architecture. See Figure 13, and corresponding text in Col. 11, lines 31, et Seq. for the disclosure of several logic states 1001-1 to 1001-n, therefore the boundary-scan architecture has a first logic state. See Col. 13, lines 30 et Seq. for the disclosure of the test port 717 shifts an instruction into the instruction register via appropriate cycles at the beginning of the Select-Instruction Register-Scan state to select control registers. Since the instruction is shifted then the number of cycles must be greater than the number of bits of the serial connection of the registers, therefore the reference disclose a number of cycles greater than the number of bits of the serial connection.)

following supply of said serial signal, supplying to the test access port for communication to the boundary-scan architecture a start bit having a second logic state opposite to said first logic state followed by a predetermined number of data bits (See the Abstract for the disclosure of a test access port for communication to a boundary-scan architecture. See Col. 14, lines 1 et Seq for the disclosure a start bit which is the bit that will take the snoopy test port into a Reset State

in the end of Step 8. The Snoopy test port is in a Reset State (or logic state one) and the test bus is in a Run Test/Idle State (logic state two opposite of logic state one). Step 8 is dependent of the data register (containing a predetermined number of data bits) state);

at said selected module detecting said start bit and storing said predetermined number of data bits (See Col. 14, lines 1 et Seq. for Update-Data Register State which stores data bits in the Data Register).

As per Claim 2, Bhattacharya discloses the step of storing said predetermined number of data bits consists of storing said predetermined number of data bits in a program visible data register (See Col. 14, lines 1 et Seq. for Update-Data Register State which stores data bits in the Data Register, this register is a program visible data register).

As per Claim 3, Bhattacharya discloses a selected module, interpreting said predetermined number of data bits as an instruction and performing a function corresponding to said instruction (See Figure 12, and text in Col. 9, lines 59 et Seq. for the disclosure of the state diagram of the snoopy test port. The test port controller transits from the Update-Instruction Register state 226 to performing the function corresponding to the instruction in the Run Test/Idle state 202).

As per Claim 4, Bhattacharya discloses a selected module, supplying a serial signal having said first logic state to following registers in the serial connection of the plurality of registers during a first time interval and supplying to following registers in the serial connection of the plurality of registers a start bit having a second logic state opposite to said first logic state followed by said predetermined number of data bits (See Figure 1. and corresponding text in Col. 3, lines 18 et Seq., for the serial connection of a plurality of registers ICBSR 705, CBSR 725,

and CBSR 735 in a first logic state. Based on the TAP1, TAP2, and TAP3, signal inputs, the second logic state may be the opposite of the first logic state, for example with the execution of the RESET signal followed by a predetermined number of data bits in the registers).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chung, U.S. Patent No. 6,446,230 disclose a mechanism for enabling boundary scan in embedded core designs with Test Access Ports.

Landis, D.L.; Singh, P., "Optimal placement of IEEE 1149.1 test port and boundary scan resources for wafer scale integration," Proceedings of the International Test Conference, 1990 Pages: 120 -126.

Fitch, K.D.; Kane, J., "Application of boundary-scan and full-chip BIST to a 3 ASIC chip set," Proceedings of the IEEE 1991 Custom Integrated Circuits Conference, 1991, Pages: 17.5/1 -17.5/4.

Andrews, J., "An embedded JTAG, system test architecture," Electro/94 International Conference Proceedings. Combined Volumes, 199, Page(s): 691 –695.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samarina Makhdoom whose telephone number is 703-305-7209. The examiner can normally be reached on Full Time on Tuesday, Thursday, Friday, and Sunday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J. Teska can be reached on 703-305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0040 for regular communications and 703-305-0040 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

SM
October 8, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER